AMENDMENT

To the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-9 (canceled)

10. (currently amended) A semiconductor structure comprising a substrate having an active region of a first conductive type including a channel region and a non-channel region surrounding the channel region, at least a first trench and a second trench disposed in the active region, the structure comprising:

a thin insulating layer disposed over said first and second ~~trench~~ trenches partially filling said first and second ~~trench~~ trenches and being conformal to said first and second ~~trench~~ trenches;

a gate electrode comprising a first conductive vertical portion, a second conductive vertical portion and a horizontal conductive portion, wherein the conductive first vertical portion is embedded inside the first trench over ~~and~~ said thin insulating layer such that said insulating layer and said first conductive vertical portion within the first trench completely fills the first trench, the second conductive vertical portion is embedded inside the second trench over ~~and~~ said thin insulating layer such that said insulating layer and said second conductive vertical portion within the ~~first~~ second trench completely fills the second trench, and the horizontal conductive portion is disposed over the substrate and connects said first and second conductive vertical portions together; and

a first shallow doped region within the substrate disposed at an upper corner adjacent to the first conductive vertical portion and a second shallow doped region disposed at an upper corner adjacent to the second conductive vertical portion of the electrode; and

a first deep source region extending from the first shallow doped region and a second deep drain region extending from the second shallow doped region are disposed in a region within the substrate deeper than the first and second trenches.

11. (previously presented) The structure according to claim 10, wherein the thin insulating layer is formed by thermal oxidation.

12. (previously presented) The structure according to claim 10, wherein a thickness of the thin insulating layer is about 0.1 μm.

13. (currently amended) A semiconductor structure comprising a substrate having an active region of a first conductive type including a channel region and a non-channel region surrounding the channel region, at least a first trench and a second trench disposed in the active region, the structure comprising:

a thin insulating layer disposed over said first and second ~~treneh~~ trenches, the thin insulating layer being conformal to said first and second ~~treneh~~ trenches; and

a gate electrode comprising a first conductive vertical portion, a second conductive vertical portion and a horizontal conductive portion, wherein the first conductive vertical portion is embedded inside the first trench over ~~and~~ said thin insulating layer such that said thin

insulating layer and said first conductive vertical portion within the first trench completely fills the first trench, the second conductive vertical portion is embedded inside the second trench over ~~and~~ said thin insulating layer such that said thin insulating layer and said second vertical portion within the second trench completely fills the second trench, and the horizontal conductive portion is disposed over the substrate and connects said first and second conductive vertical portions together.

14. (previously presented) The structure according to claim 13, wherein the thin insulating layer is formed by thermal oxidation.

15. (previously presented) The structure according to claim 13, wherein a thickness of the thin insulating layer is about 0.1 μm.

Claims 16-18 (canceled)